

ABSTRACT

Ferroelectric memory devices and methods are provided, wherein a cell
plateline signal is applied to a ferroelectric target cell capacitor and a zero
5 cancellation capacitor is coupled with a bitline during a memory read operation.
A negative pulse is applied to the zero cancellation capacitor during the cell
plateline pulse to reduce the voltage on the bitline, thereby facilitating reduced
cell plateline voltage levels while still allowing a high percentage of the
ferroelectric saturation voltage to be applied across the ferroelectric cell
10 capacitor.